



**IAR Embedded
Workbench**

IAR Debug Probes User Guide

I-jet™ and I-jet Trace

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I-jet

- Introduction
- Working with I-jet
- Technical specifications

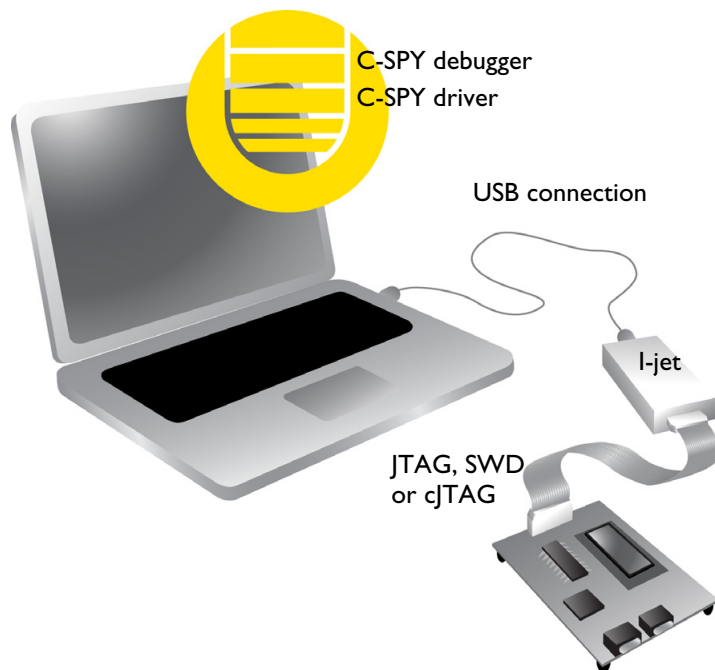
Introduction

These topics are covered:

- The I-jet in-circuit debugging probe
- Requirements
- Supported core families
- Target connections

THE I-JET IN-CIRCUIT DEBUGGING PROBE

I-jet connects to the target board via a JTAG, SWD, or cJTAG connection, and to the host computer via the USB port.



I-jet communicates using USB 2.0. (USB 1.0 is also supported but not recommended.) The I-jet in-circuit debugging probe is also referred to as a debug probe, debug adapter, or JTAG in-circuit emulator by different tool vendors.



I-jet streams power measurement data to the host computer to provide a view into program execution in real time. (**IAR Embedded Workbench for Arm:** I-jet also streams the program counter and variables.) Besides the typical JTAG debugging, I-jet is capable of providing power to the target board and measuring it with sufficient accuracy to provide a power profile during program execution in real time. This feature is referred to as *power debugging*.

For debugging Arm Cortex devices, I-jet also supports the SWO (Serial Wire Output) feature, which can be used for tracing the program execution and tracking variables at predefined points in your code.

IAR Embedded Workbench for Arm: The I-jet in-circuit debugging probe has full support for on-chip trace—ETB (Embedded Trace Buffer), MTB (Micro Trace Buffer), and TMC (Trace Memory Controller).

REQUIREMENTS

I-jet needs to be controlled by the IAR C-SPY® Debugger which comes with IAR Embedded Workbench®.

SUPPORTED CORE FAMILIES

These Arm cores are currently supported:

- Arm7
- Arm9
- Arm11
- Cortex-M
- Cortex-R
- Cortex-A

All RISC-V cores that are supported by IAR Embedded Workbench for RISC-V can be debugged using I-jet.

TARGET CONNECTIONS

These interfaces are supported:

- MIPI-20 (part number SHF-110-01-L-D): JTAG, cJTAG, SWD, SWO, ETM
- MIPI-10 (part number SHF-105-01-L-D): JTAG, cJTAG, SWD, SWO
- ARM-20 (part number HTST-110-01-L-DV): JTAG, cJTAG, SWD, SWO
- Digilent Pmod™: JTAG, cJTAG (via adapters)

I-jet comes with a MIPI-20 connector on the front panel, with MIPI-20 and MIPI-10 cables.

All other available I-jet adapters are also compatible with I-jet Trace.

Working with I-jet

These tasks are covered:

- Setup and installation
- Connecting the target system
- Updating the probe firmware

For information about debugging using I-jet, see the *C-SPY® Debugging Guide*.

SETUP AND INSTALLATION

Software

Before you can use the probe, you need to install IAR Embedded Workbench. For information, see the *Installation and Licensing Quick Reference Guide* and the *Licensing Guide*.

Probe setup

I-jet probes do not require any special driver software installation. Normally, all drivers are automatically installed as part of the IAR Embedded Workbench installation.

If you need to install the USB driver manually, navigate to:

IAR Embedded Workbench for Arm:

```
\Program Files\IAR Systems\Embedded Workbench x.x\arm\drivers\jet  
\USB\64-bit (or USB3)
```

IAR Embedded Workbench for RISC-V:

```
\Program Files\IAR Systems\Embedded Workbench x.x\riscv\drivers\i  
jet\USB\64-bit (or USB3)
```

Start the `dpinst.exe` application. This will install the USB driver.

The USB LED will flash twice after enumerating on the USB2 ports, and three times on USB3 ports.

For information about using multiple I-jet probes on the same host computer, see the *C-SPY® Debugging Guide*.

CONNECTING THE TARGET SYSTEM

Power-up your I-jet probe

- 1 Connect I-jet to the target board using the cable that matches the target board connector (MIPI-20 or MIPI-10). If an ARM-20 JTAG connector is used, you must first plug the ADA-MIPI20-ARM20 adapter into the JTAG connector.
- 2 Connect I-jet to the host computer using the USB micro cable.

Note: No harm is done if the above order is reversed.



To prevent damage, the target GND and the USB host GND must be at the same level. When *hot-plugging*, make sure that the PC and the target board power supply are connected to the same grounded wall outlet or a common grounded desktop power strip.

Power up your evaluation board

If you have an evaluation board that is prepared for it, you can power the board via I-jet through pin 19 on the standard ARM-20 connector, or pin 11/13 on the small MIPI-20 connector. Target power of up to 420 mA can be supplied from I-jet with overload protection. Most of the IAR KickStart Kits contain an evaluation board that can be powered this way. Make sure that the power jumper found on most of these boards matches your setup.

Note: The target board will get power via I-jet once you choose the **Download and Debug** or **Debug without Downloading** command, but not before.

Note: The only way to use the power debugging feature is to power up your evaluation board via I-jet.

UPDATING THE PROBE FIRMWARE

I-jet and I-jet Trace are designed so that firmware updates are not necessary unless new features added to IAR Embedded Workbench require extra hardware support. When a new version of IAR Embedded Workbench is released and a new feature that requires new firmware is used, C-SPY displays a message in the **Debug Log** window asking you to update the firmware.

Note: Support for new MCU devices is managed by software updates in IAR Embedded Workbench, and has nothing to do with I-jet or I-jet Trace firmware.

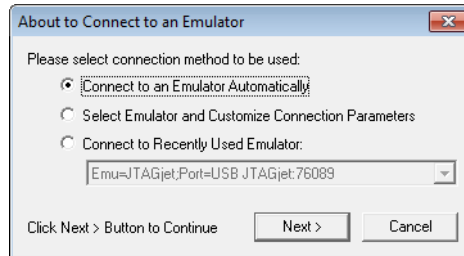
For more information about firmware versions, see the release notes.



Make sure that you do not accidentally disconnect the probe during the update process, as this can damage the probe permanently.

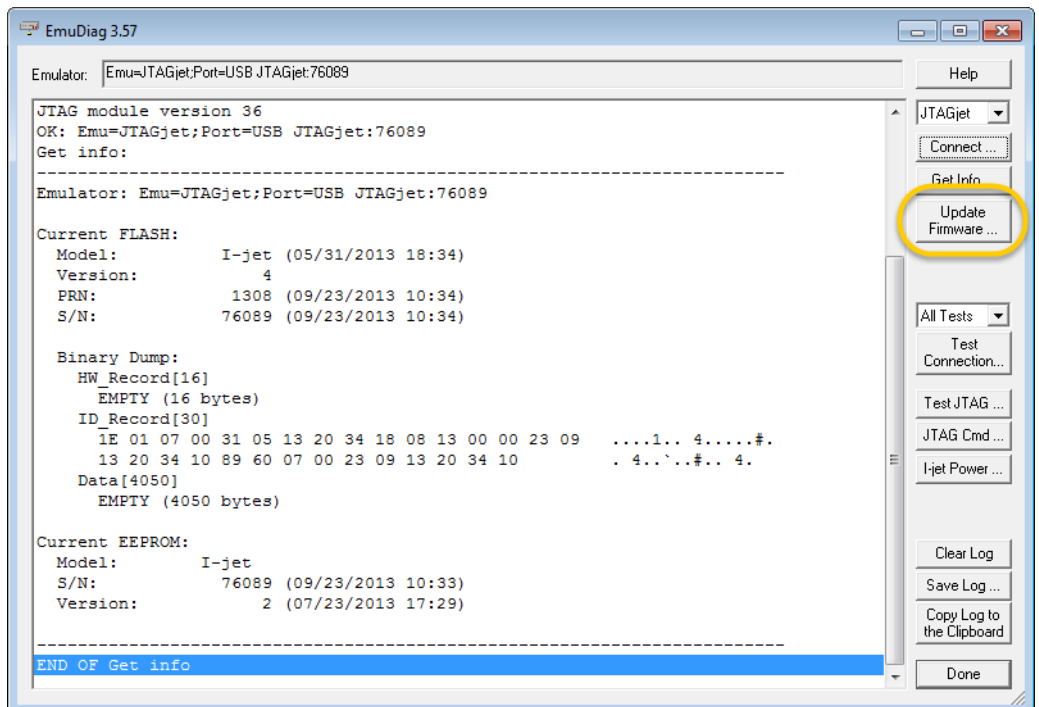
To update the probe firmware:

- 1 In IAR Embedded Workbench, choose **I-jet>EmuDiag** to display the **About to Connect to an Emulator** dialog box.



Select **Connect to an Emulator Automatically** and click **Next**.

- 2 In the **EmuDiag** dialog box, click **Update Firmware**.

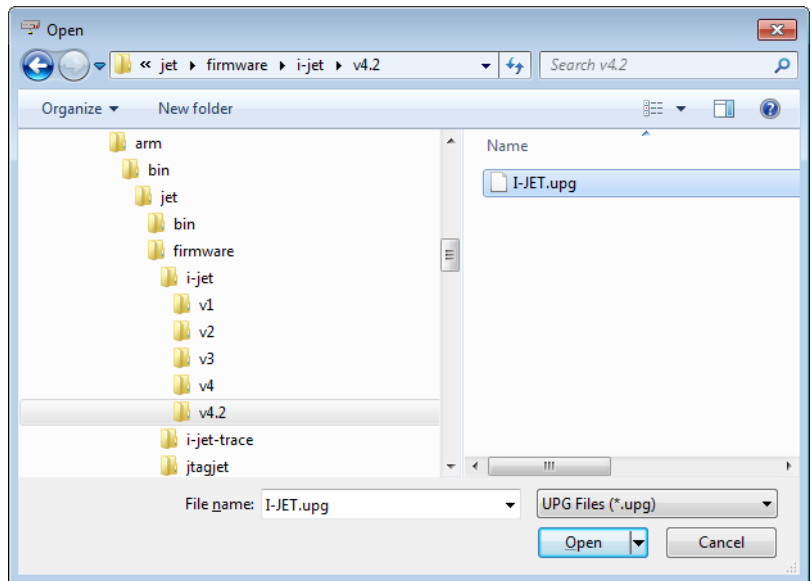


3 In the **Open** dialog box, browse to this folder of your IAR Embedded Workbench installation:

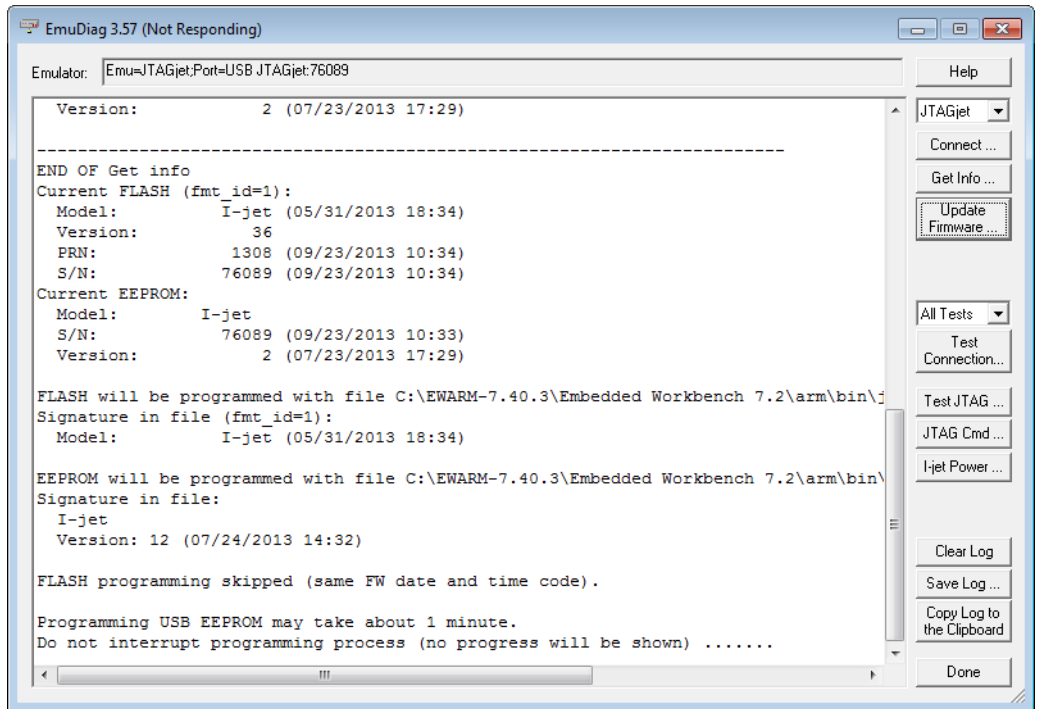
IAR Embedded Workbench for Arm: arm\bin\jet\firmware\i-jet

IAR Embedded Workbench for RISC-V: riscv\bin\ijet\firmware\i-jet

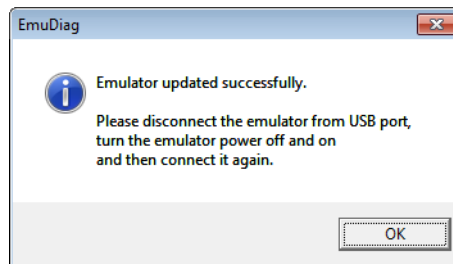
In one of the subfolders, select the firmware file that you want to use and click **Open**.



4 The update log information is displayed in the **EmuDiag** dialog box.



5 When the firmware update is complete, a message is displayed.



Technical specifications

Reference information about:

- *Model specifications*, page 13
- *JTAG timing specification*, page 14
- *Hardware revision history*, page 15
- *Target interface*, page 15
- *Indicators*, page 19
- *Adapters*, page 20

MODEL SPECIFICATIONS

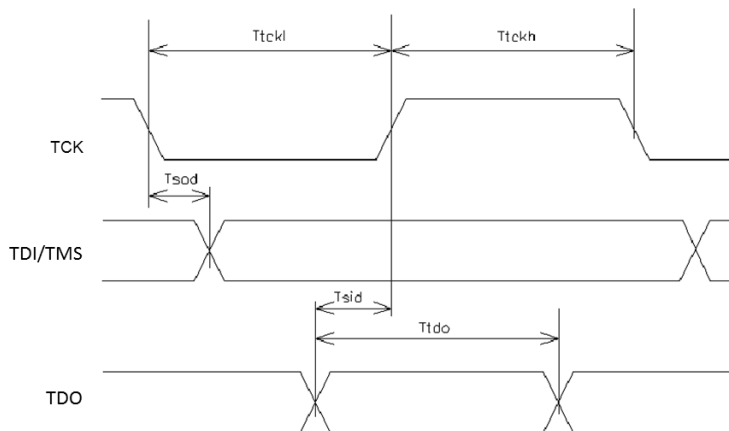
These are the specifications of I-jet:

USB speed	480 Mbps (USB 2.0)
USB connection	Micro-B
Target connection	MIPI-20, MIPI-10
I-jet debug interface	JTAG, SWD, and cJTAG
JTAG/SWD maximum clock	32 MHz
SWO protocols supported	Manchester and UART
SWO maximum speed	60 Mbps
Power supplied to target	420 mA max at 4.4 V-5 V
Over-current protection	~520 mA
Target power measurement resolution	~160 μ A
Target power measurement speed	up to 200 ksps (kilo samples per second)
JTAG voltage range (auto-sensing)	1.65 V to 5.5 V
JTAG VTref measurement resolution	~2 mV
Current draw from VTref	< 50 μ A
JTAG clock rise/fall time (TCK)	<= 2 ns*
Clock fall time	<= 2 ns*

* <= 4 ns when the target board is connected

JTAG TIMING SPECIFICATION

This figure shows the JTAG timing and parameters:



In a JTAG device that fully complies to IEEE1149.1 standard, the TDI/TMS signals should be sampled on the rising edge of TCK, and TDO should be sent on the falling edge of TCK. I-jet takes advantage of these requirements and changes its TDI and TMS signals on the falling edge of TCK and samples the TDO on the rising edge of TCK. However, to accommodate target boards with long JTAG chains and fast JTAG clocks, I-jet allows TDO to be as late as 50 ns after the rising edge of TCK.

IAR Embedded Workbench for Arm: In the adaptive mode of operation, I-jet samples the TDO on the rising edge of RTCK rather than TCK.

This table shows the timing specifications of the JTAG port measured at the end of its MIPI-20 cable without connection to target (VTref set to 3.3 V). The only load on the measured signals is the oscilloscope 3.9 pF probe.

Parameter	Min	Max	Description
T_{tckl}	15.6 ns	250 us	TCK LOW period
T_{tckh}	15.6 ns	250 us	TCK HIGH period
T_{sod}^1	--	2.0 ns	TDI and TMS outputs valid from TCK falling
T_{sid}^2	3 ns before TCK to 50 ns after TCK	--	TDO setup to TCK rising

Table 1: I-jet JTAG port timing specifications

Parameter	Min	Max	Description
T_{tdo}	T_{tckl}	--	TDO valid length

Table 1: I-jet JTAG port timing specifications (Continued)

1 T_{sod} is the maximum delay from the falling edge of TCK and a valid level on the I-jet output signals, TDI and TMS. The target MCU will sample these signals on the following rising edge of TCK and so the minimum setup time for the target, relative to the rising edge of TCK, is $T_{tckl} - T_{sod}$.

2 T_{sid} is the minimum setup time for the TDO input signal, relative to the rising edge of TCK when I-jet samples this signal. Because the target MCU changes its TDO value on the previous falling edge of TCK, there might not be enough time at very-high JTAG speeds for the TDO to arrive before the positive edge of TCK. To compensate for any TDO delays, I-jet configures itself automatically to delays introduced to the TDO by the target board and will tolerate TDO delays of up to 50 ns after the positive edge of the TCK.

HARDWARE REVISION HISTORY

These are the versions of I-jet:

Version	Change specification	Date
Version A	The first version	April 2012
Version B	Added extra RAM to the SWO FIFO buffer to improve SWO performance on older, slower PCs. Optional board current measurement resolution at 16.3 uA instead of 163 uA on I-jet Version A.	June 2017

Table 2: I-jet versions

Version, production date, and serial number can be found on the backside of the probe.

Note: In IAR Embedded Workbench, choose **I-jet>EmuDiag** to start the **EmuDiag** application where you can diagnose the connection between the host computer, the probe, and the board.

TARGET INTERFACE

This section contains descriptions of pinout, signals, and connectors. The following cables are described in detail:

- The JTAG/SWD - MIPI-20 cable
- The JTAG/SWD - MIPI-10 cable

The JTAG/SWD - MIPI-20 cable

I-jet comes with a 6-inch cable with 20-pin MIPI connectors on both ends for devices with 20-pin MIPI headers. Pin 7 on each end is keyed with a white plug:

VTref	1 ●●	2	SWDIO/TMS
GND	3 ●●	4	SWCLK/TCK
GND	5 ●●	6	SWO/TDO
---	7 ●	8	TDI
GND	9 ●●	10	nRESET
TgtPwr	11 ●●	12	TRACECLK
TgtPwr	13 ●●	14	TRACEDATA[0] /SWO2
GND	15 ●●	16	TRACEDATA[1] /nTRST
GND	17 ●●	18	TRACEDATA[2]
GND	19 ●●	20	TRACEDATA[3]

The mating connector for a target board has the pitch size 0.05 in (1.27 mm). You can, for example, use part number SHF-110-01-L-D.

These are the MIPI-20 pin definitions:

Pin	Signal	Type	Description
1	VTref	Input	The target reference voltage. Used by I-jet to check whether the target has power, to create the logic-level reference for the input comparators, and to control the output logic levels to the target. It is normally fed from JTAG I/O voltage.
2	SWDIO/TMS	I/O, output	JTAG mode set input of target CPU. This pin should be pulled up on the target. Typically connected to TMS of the target CPU.
3			This pin is a GND pin connected to GND in I-jet. It should also be connected to GND in the target system.
4	SWCLK/TCK	Output	JTAG clock signal to target CPU. It is recommended that this pin is pulled to a defined state of the target board. Typically connected to TCK of the target CPU.

Table 3: MIPI-20 pin definitions

Pin	Signal	Type	Description
5			This pin is a GND pin connected to GND in I-jet. It should also be connected to GND in the target system.
6	SWO/TDO	Input	JTAG data output from target CPU. Typically connected to TDO of the target CPU. When using SWD, this pin is used as Serial Wire Output (SWO) trace port. (Optional, but not required for SWD communication.)
--	--	--	This pin (normally pin 7) does not exist.
8	TDI	Output	JTAG data input of target CPU. It is recommended that this pin is pulled to a defined state on the target board. Typically connected to TDI of the target CPU. For CPUs which do not provide TDI (SWD-only devices), this pin is not used (tri-stated).
9			This pin is a GND pin connected to GND in I-jet. It should also be connected to GND in the target system.
10	nRESET	I/O	Target CPU reset signal. Typically connected to the RESET pin of the target CPU, which is typically called nRST, nRESET, or RESET. Bidirectional pin. By default an input that detects the board's reset signal, but it can be configured as output and used for asserting a reset to the board.
11	TgtPwr	Output	This pin can be used for supplying 5 V power to the target hardware from I-jet.
12 Not used	TRACECLK	Input	Input trace clock.
13	TgtPwr	Output	This pin can be used for supplying 5 V power to the target hardware from I-jet.
14 Not used	TRACEDATA[0] / SWO2	Input	Input Trace data pin 0. This pin can be used as secondary SWO.
15			This pin is a GND pin connected to GND in I-jet. It should also be connected to GND in the target system.

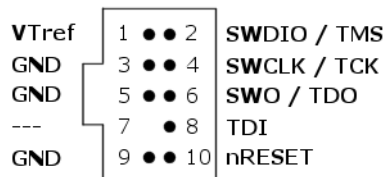
Table 3: MIPI-20 pin definitions (Continued)

Pin	Signal	Type	Description	
16	Not used	TRACEDATA[1] / nTRST	I/O	Input Trace data pin 1. This pin can be used as nTRST. When the pin is used as nTRST, the signal is an output signal.
17				This pin is a GND pin connected to GND in I-jet. It should also be connected to GND in the target system.
18	Not used	TRACEDATA[2]	Input	Input Trace data pin 2.
19				This pin is a GND pin connected to GND in I-jet. It should also be connected to GND in the target system.
20	Not used	TRACEDATA[3]	Input	Input Trace data pin 3.

Table 3: MIPI-20 pin definitions (Continued)

The JTAG/SWD - MIPI-10 cable

I-jet also comes with a 6-inch cable with a 20-pin MIPI connector on one side (to connect to I-jet) and a 10-pin MIPI connector on the other side for connection to devices with 10-pin headers. Pin 7 on each end is keyed with a white plug:



The mating connector for a target board has the pitch size 0.05 in (1.27 mm). You can, for example, use part number SHF-105-01-L-D.

These are the MIPI-10 pin definitions:

Pin	Signal	Type	Description
1	VTref	Input	The target reference voltage. Used by I-jet to check whether the target has power, to create the logic-level reference for the input comparators, and to control the output logic levels to the target. It is normally fed from JTAG I/O voltage.
2	SWDIO/TMS	I/O, output	JTAG mode set input of target CPU. This pin should be pulled up on the target. Typically connected to TMS of the target CPU.

Table 4: MIPI-10 pin definitions

Pin	Signal	Type	Description
3	GND	GND	Connected to logic GND on I-jet.
4	SWCLK/TCK	Output	JTAG clock signal to target CPU. It is recommended that this pin is pulled to a defined state of the target board. Typically connected to TCK of the target CPU.
5	GND	GND	Connected to logic GND on I-jet.
6	SWO/TDO	Input	JTAG data output from target CPU. Typically connected to TDO of the target CPU. When using SWD, this pin is used as Serial Wire Output (SWO) trace port. (Optional, not required for SWD communication.)
7	--	KEY	KEY or GND.
8	TDI/NC	Output	JTAG data input of target CPU. It is recommended that this pin is pulled to a defined state on the target board. Typically connected to TDI of the target CPU. For CPUs that do not provide TDI (SWD-only devices), this pin is not used (tri-stated).
9	GND	GND	GND and target detect presence.
10	nRESET	Output	nRESET or TRST.

Table 4: MIPI-10 pin definitions (Continued)

INDICATORS

I-jet has three LED indicators on the top, marked **TPWR**, **DBG**, and **USB**. The following indicators and their statuses are described in detail:

- The TPWR indicator (Target power)
- The DBG indicator (JTAG/SWD)
- The USB indicator

The TPWR indicator (Target power)

Indicator status	Description
Off	Power to target is not provided by I-jet.
Green	Power to target is provided by I-jet.
Yellow	Warning. Power to target is above 420 mA.
Red	Error. Overcurrent limit (520 mA) detected and power to target was switched off for protection.

Table 5: TPWR indicator statuses

The DBG indicator (JTAG/SWD)

Indicator status	Description
Off	vTref on JTAG header is too low.
Green	vTref is at or above 1.8 V.
Green blinking	Indicates JTAG/SWD communication activity.

Table 6: DBG indicator statuses

The USB indicator

Indicator status	Description
Off	No USB power.
Green steady	Initial state or no transfer.
Green blinking	USB transfers to or from I-jet.
Red blinking	USB enumeration.
Red steady	USB error, broken cable, or hardware defect. Inspect the cable and/or try a different USB port.

Table 7: USB indicator statuses

ADAPTERS

There are a number of useful adapters available. All of them are automatically recognized by I-jet. The following adapters are described in detail:

- The ADA-MIPI20-ISO isolation adapter
- The ADA-MIPI20-ARM20 adapter
- The ADA-MIPI20-TI14 adapter
- The ADA-MIPI20-cTI20 adapter
- The ADA-MIPI20-STSWD6 adapter
- The ADA-MIPI20-RISCV12 adapter

Adapters not included in the I-jet package can be purchased from IAR.

These are the mating target headers for the adapters:

TI-14	cTI-20
HTST-107-01-L-DV	TML-110-02-GD-SM-006 (shrouded)
	FTR-110-51-S-D-06 (unshrouded)

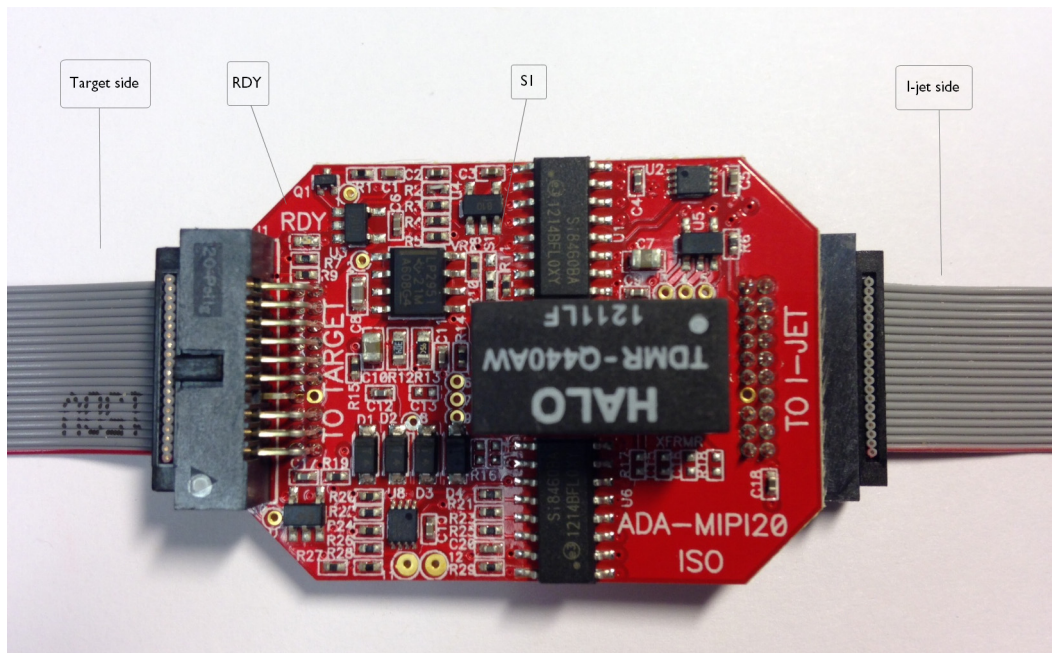
Table 8: Mating target headers, part numbers

The ADA-MIPI20-ISO isolation adapter

The ADA-MIPI20-ISO isolation adapter galvanically isolates signals between the I-jet MIPI-20 connector and the target MIPI-20 connector. You can use it to reduce the risk of damage to the I-jet debug probe associated with power ground loops, voltage spikes, electrostatic discharge (ESD), and noisy power and ground lines generated by targets which drive high-current motors and other machinery.

The adapter has two MIPI-20 headers marked **TO I-JET** and **TO TARGET**. Make sure to connect the headers correctly because switching the sides will not work and might damage the adapter. The target side of the isolation adapter can be used with any passive IAR I-jet adapters, for example, the ADA-MIPI20-ARM20, ADA-MIPI20-TI14, and ADA-MIPI20-CTI20 adapters, and the MIPI20-MIPI10 cable.

The adapter is automatically recognized by the IAR C-SPY® Debugger, and the adapter powers up and the green **RDY** LED is turned on.



Specifications

- Galvanic isolation up to 3000 V peak* (< 1 sec transients. See *Important safety and disclaimer note*, page 23) with continuous working voltage operation of up to 300 V

- Compatible with I-jet
- Supports JTAG, SWD, cJTAG, and SWO debug modes
- Compatible with I-jet Trace in JTAG, SWD, cJTAG, and SWO modes only. (ETM/N-Trace is not supported.)
- Powered entirely by I-jet via pins 11 and 13 on the MIPI-20 header
- The **RDY** LED indicates that the unit is powered and ready to use
- Supports target voltages from 2.5 to 5 V
- JTAG/SWD/cJTAG clock speed up to 32 MHz

Compatibility notes

- The adapter might not be automatically detected and powered by older versions of IAR Embedded Workbench for Arm. In such cases, select the **Target Power** option on the **Project>Options>Debugger>I-jet>Setup** page.
- The adapter does not supply power to target and therefore does not resume the target power consumption.
- When used with the ADA-MIPI20-TI14 and ADA-MIPI20-CTI20 adapters, the EMU0 and EMU1 signals are not connected.
- Due to added JTAG signals propagation delays, some target boards might not work at the full 32 MHz JTAG clock speed, so reducing the JTAG speed in C-SPY might be needed.
- The majority of Arm target boards have the SWO signal routed to pin 6 of the target MIPI20 debug connector. In cases when pin 14 is used for SWO, you must move the 0R shunt (marked S1) up from position 3-2 to position 2-1.
- The adapter does not support 1.8 V JTAG signals from target. The target JTAG voltage range is limited to 2.5-5 V.
- The JTAG interface on the target side automatically adapts to the voltage given on the target VTref pin (2.5 V-5 V). Because of the isolation barrier, the I-jet side uses its own voltage, independent of the target voltage. This is for information only and has no effect on the target JTAG operation.
- ETM trace is not supported by this adapter.

MIPI20 connector pinout on target side

VTref	1 ●	● 2	SWDIO/TMS
GND	3 ●	● 4	SWCLK/TCK
GND	5 ●	● 6	SWO/TDO
---	7 ●	● 8	TDI
GND	9 ●	● 10	nRESET
GND	11 ●	● 12	RTCK
GND	13 ●	● 14	SWO2
GND	15 ●	● 16	nTRST
GND	17 ●	● 18	NC
GND	19 ●	● 20	NC

For more information about the signal descriptions, see *The JTAG/SWD - MIPI-20 cable*, page 16.

Important safety and disclaimer note

The continuous normal operation voltage across the isolation barrier should not exceed 300 V DC.

The isolation voltage only represents a measure of immunity to transient voltages—the probe should never be used as an element of a safety isolation system. For use with higher continuous voltages, additional isolation/insulation systems must be used in accordance with the safety standard requirements.

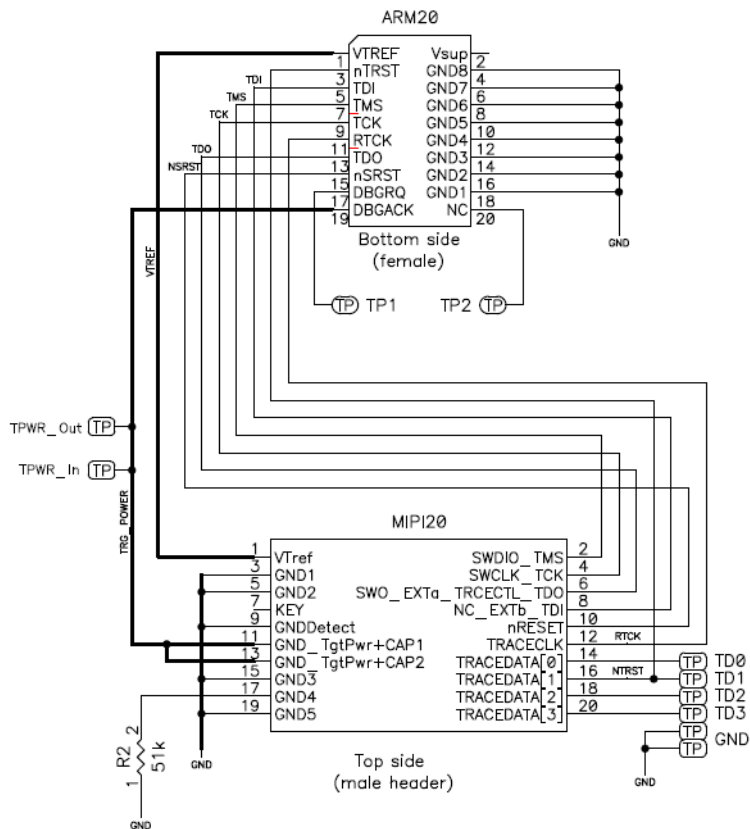


When handling equipment subjected to high voltages, use caution and follow all safety regulations. Touching any exposed circuitry on the target, the adapter, cables, or the I-jet probe can cause injury or death.

IAR or the manufacturer shall not be liable for any damages related to the use of this probe.

The ADA-MIPI20-ARM20 adapter

The ADA-MIPI20-ARM20 adapter converts the MIPI-20 I-jet cable to the legacy ARM-20—0.1 in × 0.1 in (2.54 mm × 2.54 mm) pitch—JTAG headers. This is a diagram of the adapter:



These are the pin definitions of the ADA-MIPI20-ARM20 adapter:

Pin	I-jet direction	Name	Description
nTRST	Output	Test Logic Reset	Test reset. Active LOW signal that resets the TAP controller's state machine.

Table 9: ADA-MIPI20-ARM20 adapter pin definitions

Pin	I-jet direction	Name	Description
TCK	Output	Test Clock	TCK synchronizes all JTAG transactions. TCK connects to all JTAG devices in the scan chain. TCK flows down the stack of modules and connects to each JTAG device. (IAR Embedded Workbench for Arm: However, if there is a device in the scan chain that synchronizes TCK to some other clock, then all down-stream devices are connected to the RTCK signal on that processor.)
TMS	Output	Test Mode Select	TMS controls transitions in the tap controller state machine. TMS connects to all JTAG devices in the scan chain as the signal flows down the module stack.
TDI	Output	Test Data Input	TDI is the test data input signal that is routed to the TDI input of the first device in the scan chain.
TDO	Input	Test Data Output	TDO is the return path of the test data input signal TDI. In a multi-device JTAG chain, the TDO of the first device connects to the TDI of the next device, etc. The last device's TDO is connected to the TDO on the JTAG header.
RTCK	Input	TCK Return	IAR Embedded Workbench for Arm: RTCK is a mechanism for returning the sampled clock to the JTAG equipment, so that the clock is not advanced until the synchronizing device captured the data. In adaptive clocking mode, I-jet is required to detect an edge on RTCK before changing TCK. In a multi-device JTAG chain, the RTCK output from a device connects to the TCK input of the down-stream device. If there are no synchronizing devices in the scan chain, it is unnecessary to use the RTCK signal and it is connected to ground on the target board. IAR Embedded Workbench for RISC-V: This pin is not used and is connected to ground on the target board.

Table 9: ADA-MIPI20-ARM20 adapter pin definitions (Continued)

Pin	I-jet direction	Name	Description
VTref	Input	Voltage Target Reference	This is the target reference voltage. It indicates that the target has power. VTref is normally fed from Vdd on the target hardware and might have a series resistor (though this is not recommended). VTref is used by I-jet to detect if target power is active and to set JTAG signal voltage reference for level translators.
nSRST	I/O	System Reset	Active LOW open-collector signal that is driven by I-jet to reset the device and/or the target board. I-jet senses this line to determine when you have reset the device.
Vsupply	Output	--	This pin is not connected to I-jet.
DBGRQ	Output	--	This pin is not connected on I-jet.
DBGAC K/TRGP WR	Output	Target Power	This pin is used under SW control to supply 5 V power to the target board. It should be routed through a jumper shunt to the 5 V DC board input to eliminate the power adapter during debugging. The maximum current supplied by I-jet on this pin is about 420 mA. When the supplied current reaches ~520 mA, the power will be shut down for protection.

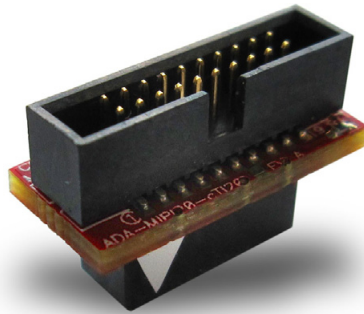
Table 9: ADA-MIPI20-ARM20 adapter pin definitions (Continued)

The R2 pull-down on pin 17 of the I-jet MIPI20 connector is a signal to I-jet that a legacy ADA-MIPI20-ARM20 adapter is being used. Other adapters will have different resistors so that I-jet can identify them if needed. A solid GND on this pin means that no adapter is being used, and that the MIPI cable is connected directly between the I-jet and the target board.

The ADA-MIPI20-TI14 adapter

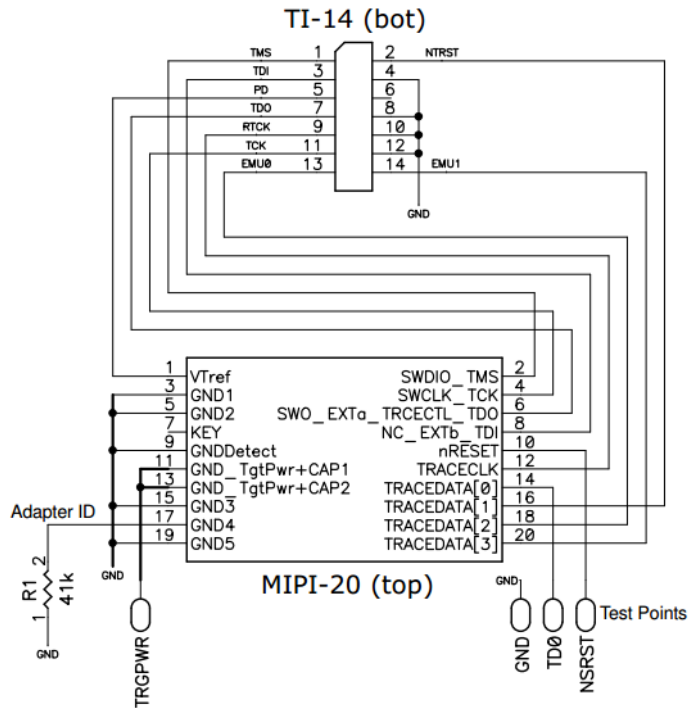
The ADA-MIPI20-TI14 adapter converts the I-jet standard MIPI-20 cable pinout to the Texas Instruments legacy 14-pin JTAG interface used on older OMAP and other TMS320, TMS470, and TMS570 target boards.

The adapter has the MIPI-20 male header on top for connecting the I-jet MIPI-20 cable and a TI-14-style female header (socket) on the bottom. The TI-14 JTAG header is a 14-pin, double-row, 0.1 in × 0.1 in (2.54 mm × 2.54 mm) pitch connector with a key (plug) in position 6 to prevent misconnections. In case the plug is missing, a white arrow on pin 1 of the TI-14 connector helps you ensure proper orientation.



This is a diagram of the ADA-MIPI20-TI14 adapter:

ADA-MIPI20-TI14

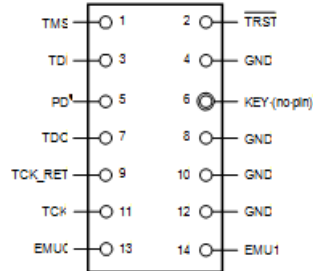


These are the pin definitions for the ADA-MIPI20-TI14 adapter:

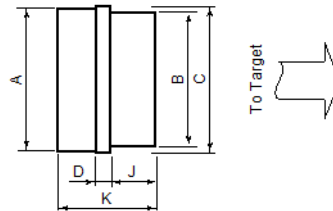
Pin	I-jet direction	Name	Description
nTRST	Output	Test Logic Reset	Active LOW signal that causes all test and debug logic in the device to be reset along with the IEEE 1149.1 TAP.
TCK	Output	Test Clock	This is the test clock used for driving the IEEE 1149.1 TAP state machine and logic.
TMS	Output	Test Mode Select	Directs the next state of the IEEE 1149.1 TAP state machine.
TDI	Output	Test Data Input	IEEE 1149.1 scan data input to the device.
TDO	Input	Test Data Output	IEEE 1149.1 scan data output from the device.
RTCK	Input	TCK Return	IAR Embedded Workbench for Arm: Used only in Adaptive Clocking mode. I-jet monitors RTCK to determine when to send the next TCK. IAR Embedded Workbench for RISC-V: Not used; connected to ground on the target board.
PD	Input	Power Detect	Should be tied to the I/O voltage of the target device. Used by I-jet to detect whether target power is active and to set the JTAG signal voltage reference for level translators.
EMU0	I/O	Emulation 0	Depending on the device, EMU pins support boot modes and other features. I-jet does not use this pin but it is routed to the TRACEDATA[2] pin on the MIPI20 connector. For proper booting, this pin should be pulled up on the target.
EMU1	I/O	Emulation 1	Depending on the device, EMU pins support boot modes and other features. I-jet does not use this pin but it is routed to the TRACEDATA[3] pin on the MIPI20 connector. For proper booting, this pin should be pulled up on the target.

Table 10: ADA-MIPI20-TI14 adapter pin definitions

This is the pinout of the target TI14 JTAG header. Pin 6 should be missing to indicate the proper orientation.



These are the top view dimensions of the ADA-MIPI20-TI14 adapter:



A	0.74 in (18.9 mm)
B	1.0 in (25.4 mm)
C	0.76 in (19.4 mm)
D	0.062 in (1.6 mm)
J	0.38 in (9.6 mm)
K	0.80 in (20.3 mm)

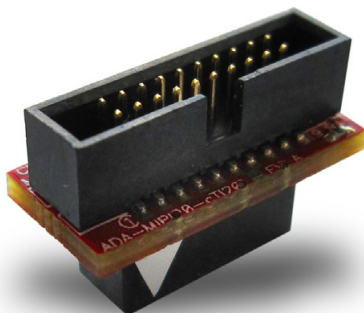
TI14 header information (for target board)

The TI14 header is manufactured by Samtec USA. The model number is TSM-107-01-F-DV. For more information, see the manufacturer's web page: <http://www.samtec.com/products/tsm>.

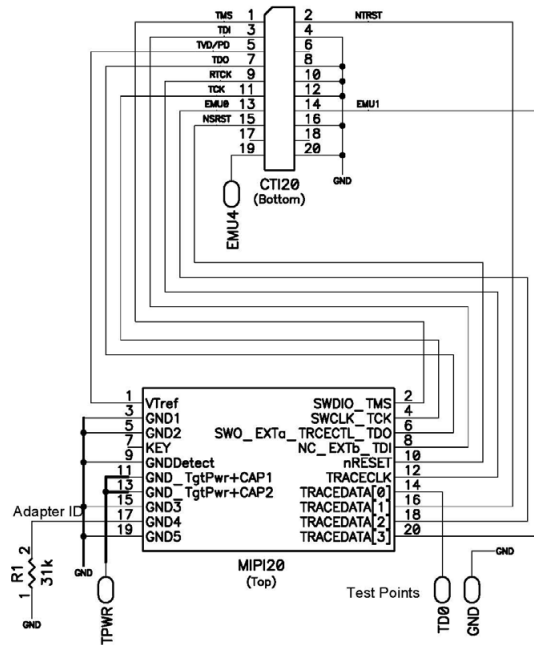
The ADA-MIPI20-cTI20 adapter

The ADA-MIPI20-cTI20 adapter adapts the I-jet standard MIPI-20 cable pinout to the Texas Instruments compact 20-pin JTAG interface used on some newer OMAP, DaVinci, and other TMS320, TMS470, and TMS570 target boards.

The adapter has the MIPI-20 male header on top for connecting the I-jet MIPI-20 cable, and a cTI-20 style female header (socket) on the bottom. The cTI-20 JTAG header is a 20-pin, double-row, high-density 0.05 in × 0.1 in (1.27 mm × 2.54 mm) pitch connector with a key (plug) in position 6 to prevent misconnections. In case the plug is missing, a white arrow on pin 1 of the cTI-20 connector helps you ensure proper orientation.



This is a diagram of the ADA-MIPI20-cTI20 adapter:



These are the pin definitions for the ADA-MIPI20-cTI20 adapter:

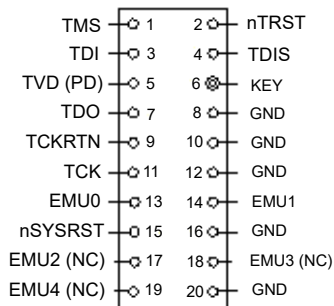
Pin	I-jet direction	Name	Description
nTRST	Output	Test Logic Reset	Active LOW signal that causes all test and debug logic in the device to be reset along with the IEEE 1149.1 TAP.
TCK	Output	Test Clock	Test clock used to drive the IEEE 1149.1 TAP state machine and logic.
TMS	Output	Test Mode Select	Directs the next state of the IEEE 1149.1 TAP state machine.
TDI	Output	Test Data Input	IEEE 1149.1 scan data input to the device.
TDO	Input	Test Data Output	IEEE 1149.1 scan data output from the device.

Table 11: ADA-MIPI20-cTI20 adapter pin definitions

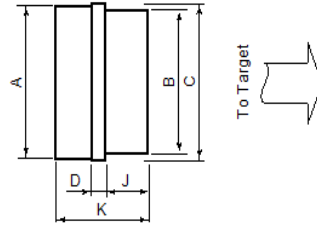
Pin	I-jet direction	Name	Description
RTCK	Input	TCK Return	IAR Embedded Workbench for Arm: Used only in Adaptive Clocking mode. I-jet monitors RTCK to determine when to send the next TCK. IAR Embedded Workbench for RISC-V: Not used; connected to ground on the target board.
PD	Input	Power Detect	Should be tied to the I/O voltage of the target device. Used by I-jet to detect if target power is active and to set the JTAG signal voltage reference for level translators.
EMU0	I/O	Emulation 0	Depending on the device, EMU pins support boot modes and other features. I-jet does not use this pin but it is routed to the TRACEDATA[2] pin on the MIPI20 connector. For proper booting, this pin should be pulled-up on the target.
EMU1	I/O	Emulation 1	Depending on the device, EMU pins support boot modes and other features. I-jet does not use this pin but it is routed to the TRACEDATA[3] pin on the MIPI20 connector. For proper booting, this pin should be pulled-up on the target.
nRESET	I/O	System Reset	Active LOW open-collector signal that can be driven by I-jet to reset the device and/or the target board. I-jet senses this line to determine when a board has been reset by the user or by watchdog timer.

Table 11: ADA-MIPI20-ct120 adapter pin definitions (Continued)

This is the pinout of the target ct120 JTAG header. Pin 6 should be missing to indicate the proper orientation.

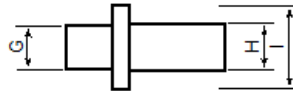


These are the top view dimensions of the ADA-MIPI20-cTI20 adapter:



A	0.74 in (18.9 mm)
B	0.7 in (17.7 mm)
C	0.76 in (19.4 mm)
D	0.07 in (1.8 mm)
J	0.24 in (6.0 mm)
K	0.50 in (12.8 mm)

These are the side view dimensions of the ADA-MIPI20-cTI20 adapter:



G	0.19 in (4.8 mm)
H	0.2 in (5.1 mm)
I	0.36 in (9.1 mm)

cTI20 header information (for target board)

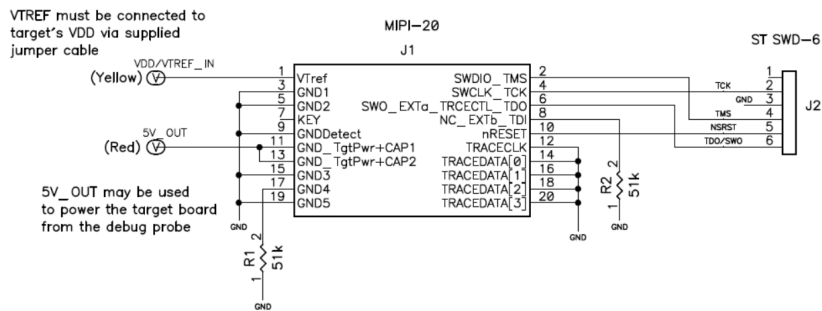
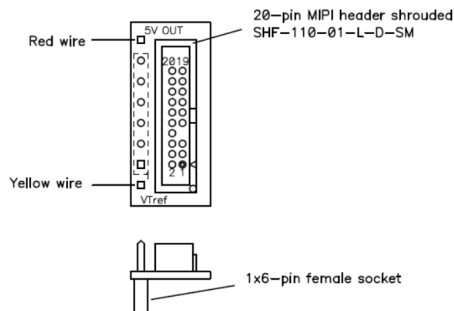
The cTI20 header is manufactured by Samtec USA. The model number is FTR-110-51-S-D-06. For more information, see the manufacturer's web page, <http://www.samtec.com/products/ftr>.

The ADA-MIPI20-STSWD6 adapter

The ADA-MIPI20-STSWD6 adapter converts the I-jet standard MIPI-20 cable pinout to the ST SWD 6-pin female connector header.

The target header has pins spaced at 0.1 in (2.54 mm). The adapter has 6-pin female connector plus two wire cables with female connectors for connecting SWD voltage reference input (VTref) and 5V_OUT to optionally power the target board from the debug probe.

This is a diagram of the ADA-MIPI20-STSWD6 adapter:



These are the pin definitions for the ADA-MIPI20-STSWD6 adapter:

Pin	I-jet direction	Name	Description
1		NC	No connection - not used.

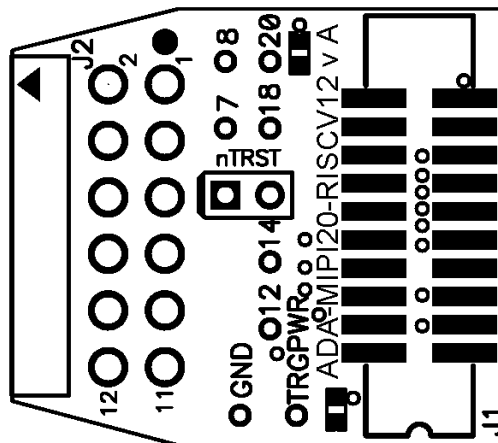
Table 12: ADA-MIPI20-STSWD6 adapter pin definitions

Pin	I-jet direction	Name	Description
2	Output	SWCLK /TCK	SWD clock signal to the target CPU. It is recommended that this pin is pulled to a defined state of the target board.
3		GND	Common ground.
4	I/O	SWIO /TMS	Bi-directional data pin for SWD. This pin should be pulled up on the target (100k recommended).
5	I/O	NSRST	System reset is open-drain and active low and should be pulled-up on the target board. Allows debug probe to reset the MCU if necessary.
6	Input	TDO /SWO	SWD trace output port. Optional—not required for SWD operation.
Yellow	Input	VTref	The target reference voltage. Used by I-jet to check whether the target has power, to create the logic-level reference for the input comparators, and to control the output logic levels to the target. It is normally fed from the target's VDD voltage.
Red	Output	5V Output	This pin can be used for supplying 5V power to the target hardware from I-jet.

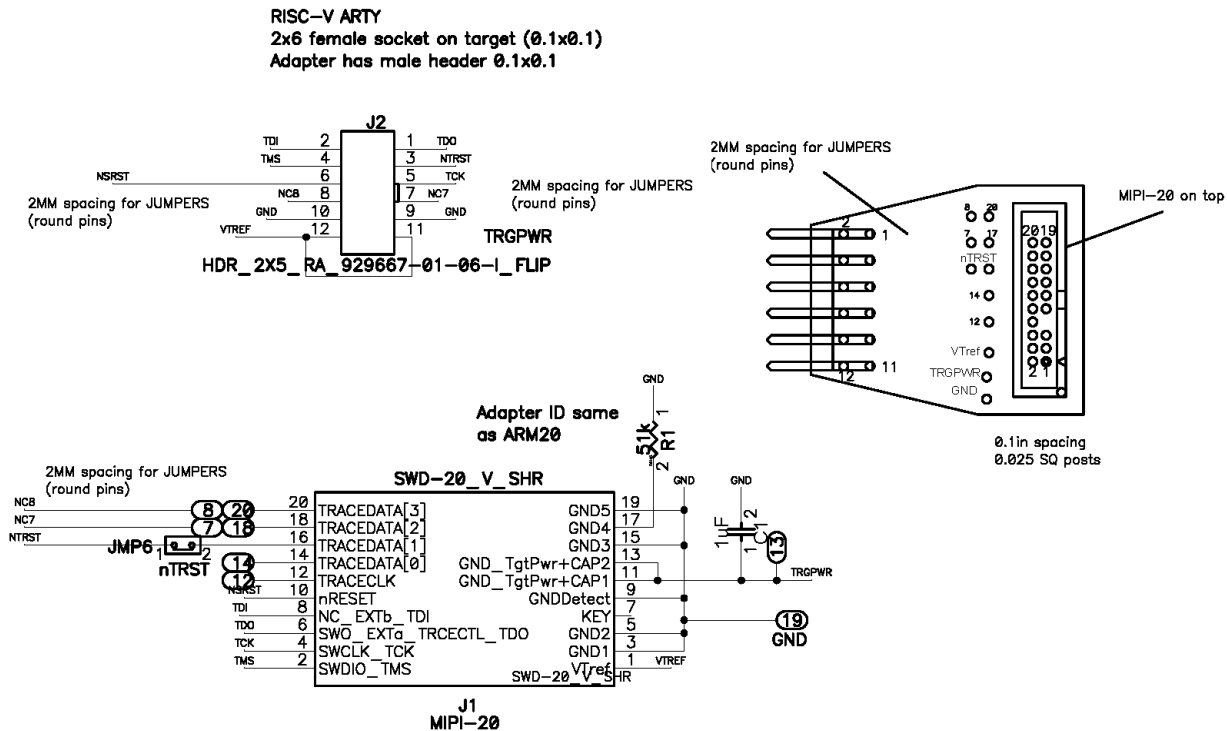
Table 12: ADA-MIPI20-STSWD6 adapter pin definitions (Continued)

The ADA-MIPI20-RISCV12 adapter

This is a pinout of the ADA-MIPI20-RISCV12 adapter:



This is a diagram of the ADA-MIPI20-RISCV12 adapter:



This is the matching between the signal names and pins of connector J2 HDR_2X6_RA_ARTY:

Signal	J1/MIPI20	J2
TDO	6	1
TDI	8	2
NTRST	16 (jumped)	3
TMS	2	4
TCK	4	5
NSRST	7	6
NC7	7 (jumped)	7
NCS	20 (jumped)	8
GND	3, 5, 9, 15, 19	9, 10

Table 13: J2 HDR_2X6_RA_ARTY signal matching

Signal	J1/MIP120	J2
VTREF	1	11,12
TRGPWR	11, 13	—
NC12	12	—
NC14	14	—

Table 13: J2 HDR_2X6_RA_ARTY signal matching (Continued)

I-jet Trace

- Introduction
- Working with I-jet Trace
- Technical specifications

Introduction

These topics are covered:

- The I-jet Trace CM and I-jet Trace A/R/M in-circuit debugging probes
- Requirements
- Target connections

THE I-JET TRACE CM AND I-JET TRACE A/R/M IN-CIRCUIT DEBUGGING PROBES

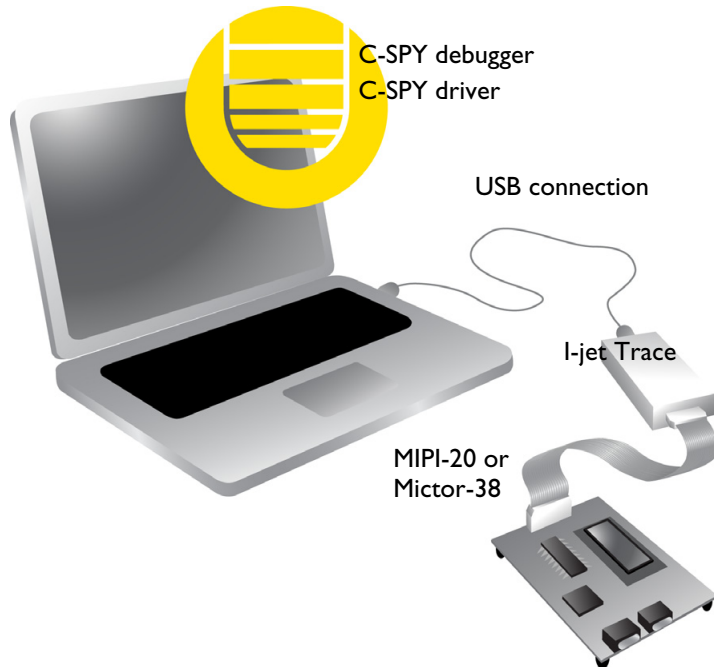
I-jet Trace CM and I-jet Trace A/R/M are in-circuit debugging probes, designed to take full advantage of the speed and current delivery of the USB3 communication ports. USB 2.0 is also supported, but not recommended due to slower speed and smaller power delivery.

I-jet Trace CM and I-jet Trace A/R/M have all the features of I-jet, but with enhanced performance and support for Arm ETM (Embedded Trace Macrocell) trace and RISC-V N-Trace (Nexus-based Trace). This allows for real-time tracing of instructions and data over a 1, 2 or 4-bit trace bus on Arm Cortex-M and RISC-V devices.

I-jet Trace A/R/M provides extensive debug and trace functionality for Arm and RISC-V. I-jet Trace A/R/M is equipped with up to 16-bit wide trace data collection. Note that Arm Cortex devices must be equipped with the CoreSight™ debug interface.

Note: Whenever I-jet Trace is mentioned in this document, both the I-jet Trace CM and the I-Jet Trace A/R/M probes are referred to, unless otherwise explicitly specified.

I-jet Trace CM connects to the target board via a MIPI-20 header. By default, I-jet Trace A/R/M connects to the target via the Mictor-38 headers, but it also supports the MIPI-20 headers. The probes connect to the host computer via the USB port.



I-jet Trace streams the program counter, variables, and power measurement data to the host computer to provide a view into program execution in real time. Besides the typical JTAG debugging, I-jet Trace is capable of providing power to the target board, and measuring it with sufficient accuracy to provide a power profile during program execution in real time. This feature is referred to as *power debugging*.

For debugging Arm Cortex devices, I-jet Trace also supports the SWO (Serial Wire Output) feature, which can be used for tracing the program execution and tracking variables at predefined points in your code.

The I-jet Trace in-circuit debugging probe is also referred to as a debug probe, debug adapter, or JTAG in-circuit emulator by different tool vendors.

REQUIREMENTS

I-jet Trace needs to be controlled by the IAR C-SPY® Debugger which comes with the IAR Embedded Workbench® IDE.

TARGET CONNECTIONS

These target interfaces are supported:

- MIPI-20, for up to 4-bit wide trace (part number SHF-110-01-L-D): JTAG, SWD, cJTAG, SWO, ETM, and N-Trace
- MIPI-10 for debugging without trace (part number SHF-105-01-L-D): JTAG, SWD, cJTAG, SWO
- ARM-20 for debugging without trace (part number HTST-110-01-L-DV): JTAG, SWD, cJTAG, SWO
- Mictor-38 for up to 16-bit wide trace (I-jet Trace A/R/M only): JTAG, SWD, cJTAG, ETM, SWO, and N-Trace
- MIPI-60 (with trace) and TI-14/cTI-20 (without trace) connections via adapters
- Digilent Pmod™ for debugging with or without trace, via adapters

I-jet Trace CM comes with a MIPI-20 connector on the front panel, and with MIPI-20 and MIPI-10 cables.

I-jet Trace A/R/M comes with an adapter board with a Mictor-38 connector that plugs directly into the target board. For boards that do not use the high-speed Mictor connector, the probe also supports the standard MIPI-20 headers.

Note: Only the MIPI-20 and Mictor-38 cables support trace functionality. All other connections (MIPI-10 and ARM-20) are only for plain JTAG/SWD/SWO/cJTAG debugging.

All I-jet adapters are compatible with I-jet Trace.

Working with I-jet Trace

These tasks are covered:

- Setup and installation
- Connecting the target system
- Using Trace
- Updating the probe firmware

For information about debugging using I-jet Trace, see the *C-SPY® Debugging Guide*.

SETUP AND INSTALLATION

Software

Before you can use the probe, you need to install IAR Embedded Workbench. For information, see the *Installation and Licensing Quick Reference Guide* and the *Licensing Guide*.

Probe setup

I-jet probes do not require any special driver software installation. Normally, all drivers are automatically installed as part of the IAR Embedded Workbench installation.

If you need to install the USB driver manually, navigate to:

IAR Embedded Workbench for Arm:

```
\Program Files\IAR Systems\Embedded Workbench x.x\arm\drivers\jet\USB\64-bit (or USB3)
```

IAR Embedded Workbench for RISC-V:

```
\Program Files\IAR Systems\Embedded Workbench x.x\riscv\drivers\ijet\USB\64-bit (or USB3)
```

Start the `dpinst.exe` application. This will install the USB driver.

The USB LED will flash twice after enumerating on the USB2 ports, and three times on USB3 ports.

For information about using multiple I-jet probes on the same host computer, see the *C-SPY® Debugging Guide*.

CONNECTING THE TARGET SYSTEM

Power-up your I-jet Trace probe

- 1 Connect I-jet Trace to the host computer using the USB3 micro cable or any other compatible high-quality USB3 cable.
- 2 Connect I-jet Trace to the target board using the cable that matches the target board connector (MIPI-20, MIPI-10, or Mictor-38). If an ARM-20 connector is used, you must first plug the ADA-MIPI20-ARM20 adapter into the JTAG connector.

Note: No harm is done if the above order is reversed.



To prevent damage, the target GND and the USB host GND must be at the same level. When *hot-plugging*, make sure that the PC and the target board power supply are connected to the same grounded wall outlet or a common grounded desktop power strip.

Supplying target power from I-jet Trace

I-jet Trace can only supply power to the target board through the MIPI-20 and ARM-20 connections. The Mictor interface does not facilitate powering targets from the debug probes.

I-jet Trace CM can supply a maximum of 4.66 V at 200 mA when using USB3 ports without the need of plugging in an external 5 V DC power supply.

I-jet Trace A/R/M must use the supplied (5 V DC at 2 A) power adapter to power a target board. When it is not powering the target, I-jet Trace A/R/M does not need the external power supply as long as it is connected to the USB3 port.

Power up your evaluation board

If you have an evaluation board that is prepared for it, you can power the board via I-jet Trace through pin 19 on the ARM-20 connector, or pin 11/13 on the small MIPI-20 connector. Target power of up to 400 mA can be supplied from I-jet Trace with overload protection. Most of the IAR KickStart Kits contain an evaluation board that can be powered this way. Make sure that the power jumper found on most of these boards matches your setup.

Note: The target board will only get power via I-Jet Trace once you choose the **Download and Debug** or **Debug without Downloading** command in C-SPY, and not before.

Note: The only way to use the power debugging feature is to power up your evaluation board via the probe.

Calibration

When the debug system powers up, the trace probe evaluates the signal quality of the trace data lines and tries to find the best sampling point for the trace data. The calibration result is displayed in the **Debug Log** window, as a visual pattern of ASCII characters.

The overall detected quality of the calibration run will be given as $q=n$, the higher, the better. It is determined by the data line with the smallest horizontal eye opening. A numbered scale corresponds to one clock phase of the detected trace clock, divided into 64 time slots. The trace clock frequency is also stated in the debug output, as $f=n\text{MHz}$.

Character	Description
+ or -	All data samples in this time slot are as expected
c	The calibration center of the data line, that is, the best sampling point found by the probe

Table 14: Trace calibration log readout

Character	Description
C	The calibration center of the data line, but also the point closest to the median for the entire calibration run
0..9%	0%..9% of the data samples have errors. (0 means that the number of errors rounds down to zero, but there are errors.)
x	10% or more of the data samples have errors
X	All data samples have errors, and a percentage cannot be computed
s	Cannot synchronize properly—no pattern is found. (The second stage of pattern detection.)
S	No zero pattern found (the first stage of pattern detection)
*	The default position of the trace clock sampling edge. This is just for orientation and for showing differences in delay of each data line.

Table 14: Trace calibration log readout (Continued)

This is an example of a calibration run:

```

-30      -20      -10      *      10      20      30      f=50.00MHz
D0: ++++++C+++++xxxxxxxxXXXXXXXXXX
D1: ++++++C+++++xxxxxXXXXXXXXXXXXX6X+
D2: ++++++C+++++3xXXxxXXXXXXXXXX
D3: ++++++C+++++0XXXXXXXXXXXXxxXX
-30      -20      -10      *      10      20      30      q=42

```

In this example, 42 out of 64 possible slots are of good quality, which should not cause any data errors during trace run. Successful trace data sampling is generally possible with a quality of at least 6.

If you need help deciphering the trace calibration log, contact IAR Technical Support.

USING TRACE

To use trace, the target board must have an Arm Cortex or a RISC-V device with the ETM/PTM/N-Trace trace pins—usually named **TraceCLK** and **TraceDxx**—and these pins must be connected to the debug connector. Because trace pins are multiplexed on some devices, take care not to connect these pins to other logic devices on the PCB to minimize the loading and improve signal integrity.

C-SPY will initialize and enable all necessary registers on the MCU to allow the ETM/N-Trace port to function properly so that no special user code instrumentation is necessary. However, ensure that the running application code does not interfere (read, write, etc.) with the GPIO pins used for the ETM/N-Trace trace.

The TRC LED on the I-jet Trace debug probe will turn green when trace data is being collected. This usually happens after trace is enabled in C-SPY and the Run command is issued.

For more information about trace, see the *C-SPY® Debugging Guide*.

UPDATING THE PROBE FIRMWARE

For more information, see *Updating the probe firmware*, page 9.

Technical specifications

Reference information about:

- *Model specifications*, page 45
- *Hardware revision history*, page 47
- *Connectors*, page 48
- *Indicators*, page 50
- *Adapters*, page 51
- *Designing target boards for trace*, page 58
- *General PCB layout guidelines*, page 59

MODEL SPECIFICATIONS

These are the specifications of I-jet Trace:

USB speed	4.8 Gbps (USB 3 SuperSpeed) 480 Mbps (USB 2.0 Hi-Speed)
USB connection	USB 3 Micro-B (USB 2.0 Micro-B-compatible)
Target connection	MIPI-20 (ETM, JTAG, cJTAG, SWO, SWD, and N-Trace) MIPI-10 (JTAG, cJTAG, SWO, and SWD) ARM-20 (JTAG, cJTAG, SWO, and SWD) Mictor-38 (I-jet Trace A/R/M only) (ETM, JTAG, cJTAG, SWO, SWD, and N-Trace)
External DC power input	5 V DC, 2 A, 0.05 in x 0.14 in (1.3 mm x 3.5 mm) (Not supplied with I-jet Trace CM)
Debug interface	ETM, JTAG, cJTAG, SWO, SWD, and N-Trace

JTAG/SWD/cJTAG maximum clock	100 MHz
JTAG/SWD clock rise & fall time	≤ 2 ns
Maximum trace clock	I-jet Trace CM: 150 MHz
SWO protocols supported	Manchester and UART
SWO sampling frequency	200 MHz
SWO maximum bandwidth	60 Mbps
Trace memory size	I-jet Trace CM: up to 256 Mbytes I-jet Trace A/R/M: up to 1 Gbyte
Power supplied to target (4.1 V-4.6 V)	400 mA max with USB 3 ports 200 mA with USB 2 ports 400 mA with ExternalDC power 600 mA (I-jet Trace A/R/M only)
Over-current protection	~420 mA with USB 3 ~220 mA with USB2 ~620 mA with ExternalDC power (5 V at 2 A)
Target power measurement resolution	~160 μ A
Target power measurement speed	up to 200 ksp/s (kilo samples per second)
JTAG/SWD/trace voltage range	1.2 V to 5 V
Current draw from target V_{Tref}	< 50 μ A
Power requirement	3000 mW maximum (from USB or external DC, without target)
Operating temperature	32-86°F (0-30°C)
Storage temperature	32-176°F (0-80°C)

I-Jet Trace A/R/M features

In addition to the above model specifications, I-jet Trace A/R/M has these features:

- Support for ETMv3, ETMv4, and PTM/PFT trace and debug interfaces on any Arm Cortex-A/R/M device equipped with CoreSight
- Trace port support of up to 350 MHz double data rate (DDR) (700 Msamples/s for each trace data line) for a total of 11.2 Gbit/s throughput
- Support for streaming of trace data at up to 3.2 Gbytes/s
- Automatic alignment of parallel trace data skew on individual bits to compensate for PCB layout and signal integrity problems
- Automatic trace data and clock voltage threshold adjustments to get the most reliable trace data collection with noisy or unterminated target boards
- 64-bit timestamp with 5 ns resolution (or CPU cycle accurate) for precise timing analysis
- 16-bit wide trace for Arm and RISC-V devices
- No external power adapter needed when powering target boards that take less than 200 mA

HARDWARE REVISION HISTORY

These are the versions of I-jet Trace CM:

Version	Change specification	Date
Version A	IAR internal version	24/Mar/2014
Version B	Production version	26/May/2014
Version C	Added 100k pull-up on nSRST	26/Nov/2014
Version C I	Increased voltage level on JTAG output pins for better compatibility with 5 V devices	15/May/2015
Version D0	No functional changes (PCB changes only)	19/Feb/2016
Version D I	No functional changes (PCB changes only)	28/Jul/2016

Table 15: I-jet Trace CM versions

These are the versions of I-jet Trace A/R/M:

Version	Change specification	Date
Version A	Production version	15/Dec/2015
Version B	No functional changes (PCB changes only)	04/Feb/2016

Table 16: I-jet Trace A/R/M versions

The version and serial number can be found on the backside of the probe. The I-jet Trace A/R/M also has the production date printed on the label.

Note: In IAR Embedded Workbench, choose **I-jet>EmuDiag** to open the **EmuDiag** application where you can diagnose the connection between the host computer, the probe, and the board.

CONNECTORS

External power

I-jet Trace has a small—0.05 in x 1.4 in (1.35 mm × 3.5 mm)—external power connector right next to the USB connector. It can be used whenever the host computer is unable to deliver the necessary power to I-jet Trace and to the target board. The external power supply must deliver 5 V DC at 1 A minimum for I-jet Trace CM and 2 A minimum for I-jet Trace A/R/M.

When external power is connected, almost all power will be taken from the external power supply, allowing more power-consuming targets (up to 600 mA) to be powered by I-jet Trace.

I-scope connector

The I-scope connector on the side of the probe is provided for connecting the legacy I-scope analog probe to the I-jet Trace.

Expansion connector

This 30-pin connector is reserved for future use to add more functionality and features to I-jet Trace.

Target connector

I-jet Trace CM comes with a MIPI-20 connector that allows a standard 20-pin flat cable (included) to connect to a target with a MIPI-20 male header. This target connection allows for JTAG/SWD/cJTAG debugging as well as 1, 2, or 4-bit ETM/N-Trace, or SWO trace.

The MIPI-20 pinout for I-jet Trace CM is the same as for I-jet.

I-jet Trace A/R/M comes with two 60-pin flat cables that terminate in an adapter board with a Mictor-38 male connector that is designed to plug in directly into the target board.

The Mictor connector allows for JTAG/SWD/cJTAG/SWO debugging as well as for up to 16-bit wide ETM or N-Trace trace.

The adapter board also contains a standard MIPI-20 header for connecting to target boards without the Mictor connection.

This is the Mictor-38 pinout for I-jet Trace A/R/M:

Signal	Pin	Pin	Signal
	1	2	
	3	4	
GND	5	6	TRACECLK
TRIGIN	7	8	TRIGOUT
nSRST	9	10	EXTTRIG
TDO	11	12	VTREF
RTCK	13	14	VSUPPLY (not used)
TCK	15	16	TRACEDATA[07]
TMS	17	18	TRACEDATA[06]
TDI	19	20	TRACEDATA[05]
nTRST	21	22	TRACEDATA[04]
TRACEDATA[15]	23	24	TRACEDATA[03]
TRACEDATA[14]	25	26	TRACEDATA[02]
TRACEDATA[13]	27	28	TRACEDATA[01]
TRACEDATA[12]	29	30	
TRACEDATA[11]	31	32	
TRACEDATA[10]	33	34	
TRACEDATA[09]	35	36	TRACECTL
TRACEDATA[08]	37	38	TRACEDATA[00]

Table 17: The Mictor-38 pinout for I-jet Trace A/R/M

The mating connector for Mictor-38 on target board is AMP/Tyco 5767054-1.



INDICATORS

I-jet Trace has four LED indicators on the top, marked **TRC**, **TPWR**, **DBG**, and **USB**. The following indicators and their statuses are described in detail:

- The TRC indicator
- The TPWR indicator (Target power)
- The DBG indicator (JTAG/SWD/cJTAG)
- The USB indicator

The TRC indicator

Indicator status	Description
Off	No trace.
Green	Collecting trace data and trace clock is present.
Red	Trace data collection is enabled but the trace clock is not present.
Orange blinking	Collecting SWO trace data.

Table 18: TRC indicator statuses

The TPWR indicator (Target power)

Indicator status	Description
Off	Power to target is not provided by I-jet.
Green	Power to target is provided by I-jet.
Yellow	Warning. Power to target is close to the overcurrent limit.
Red	Error. Overcurrent limit detected and power to target was switched off for protection.

Table 19: TPWR indicator statuses

The DBG indicator (JTAG/SWD/cJTAG)

Indicator status	Description
Off	vTref on JTAG header is too low.
Green	vTref is at or above 1.2 V.
Green blinking	Indicates JTAG/cJTAG/SWD communication activity from the target

Table 20: DBG indicator statuses

The USB indicator

Indicator status	Description
Off	No USB power.
Green steady	Initial state or no transfer.
Green blinking	USB transfers to or from I-jet Trace.
Red blinking	USB enumeration.
Red steady	USB error, broken cable, or hardware defect. Inspect the cable and/or try a different USB port.

Table 21: USB indicator statuses

ADAPTERS

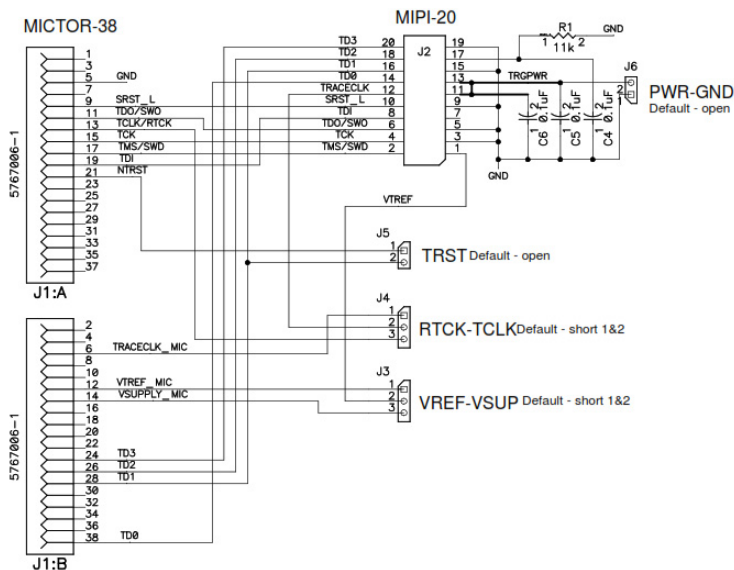
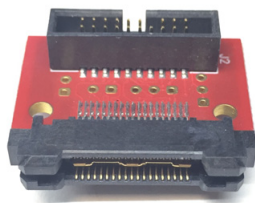
The following adapters are described in detail:

- The ADA-MIPI20-MICTOR adapter
- The ADA-MICTOR-MIPI60 adapter
- The ADA-MIPI20-RISCV24 adapter

The ADA-MIPI20-MICTOR adapter

The ADA-MIPI20-MICTOR adapter converts the I-jet Trace CM standard MIPI-20 cable pinout to the high-speed Mictor 38-pin trace connector used on some target boards.

The adapter has the MIPI-20 male header on top for connecting the I-jet Trace CM MIPI-20 cable and the Mictor-style male header that straddles the edge of the PCB. This Mictor connector (AMP/Tyco 576006-1) mates with target boards with a female Mictor connector with pitch size 0.025 in (0.064 mm). You can, for example, use AMP/Tyco 5767054-1. These connectors are keyed to prevent incorrect insertion.



Signal	Pin	Pin	Signal
	1	2	
	3	4	
GND	5	6	TRACECLK
	7	8	
nSRST	9	10	
TDO	11	12	VTREF
RTCK*	13	14	VSUPPLY
TCK	15	16	
TMS	17	18	
TDI	19	20	
nTSRST*	21	22	
	23	24	TD[3]
	25	26	TD[2]
	27	28	TD[1]
	29	30	
	31	32	
	33	34	
	35	36	
	37	38	TD[0]

Table 22: ADA-MIPI20-MICTOR adapter pinout

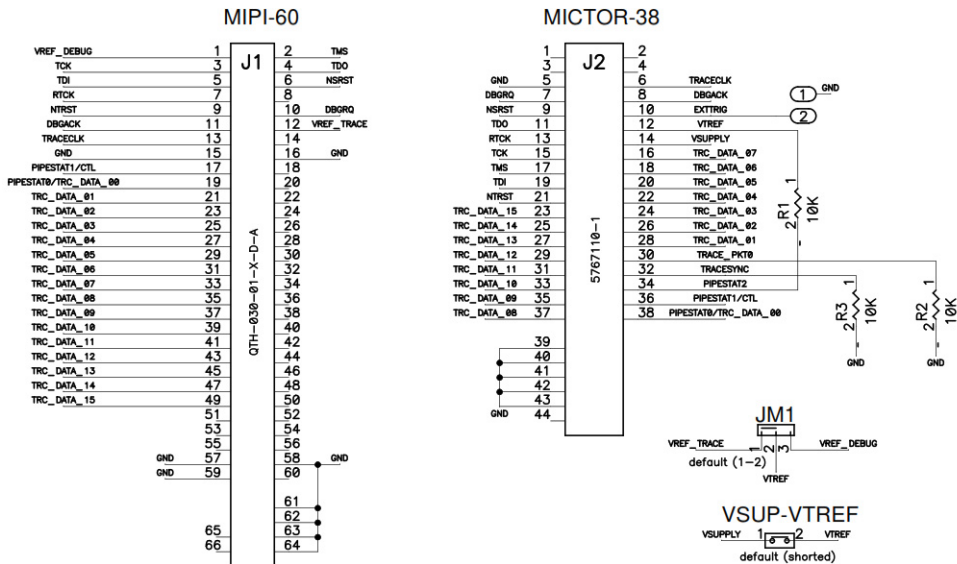
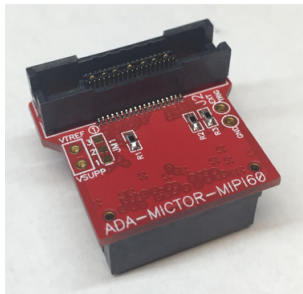
* The function of these pins is determined by the jumpers on the adapter.

The ADA-MICTOR-MIPI60 adapter

The ADA-MICTOR-MIPI60 adapter converts the I-jet Trace A/R/M standard Mictor-38 pinout to the MIPI-60 trace connector used on some target boards. The adapter has the Mictor-38 female connector on top for connecting the I-jet Trace A/R/M and the MIPI-60-style male header on the bottom.

This MIPI-60 connector (Samtec QTH-030-01-F-D-A) mates with target boards with a female MIPI-60 connector with the pitch size 0.5 mm (0.19 in). You can, for example,

use Samtec QSH-030-01-F-D-A. These connectors are keyed to prevent incorrect insertion.



Signal	Pin	Pin	Signal
VREF DEBUG	1	2	TMS
TCK	3	4	TDO
TDI	5	6	nSRST
RTCK	7	8	

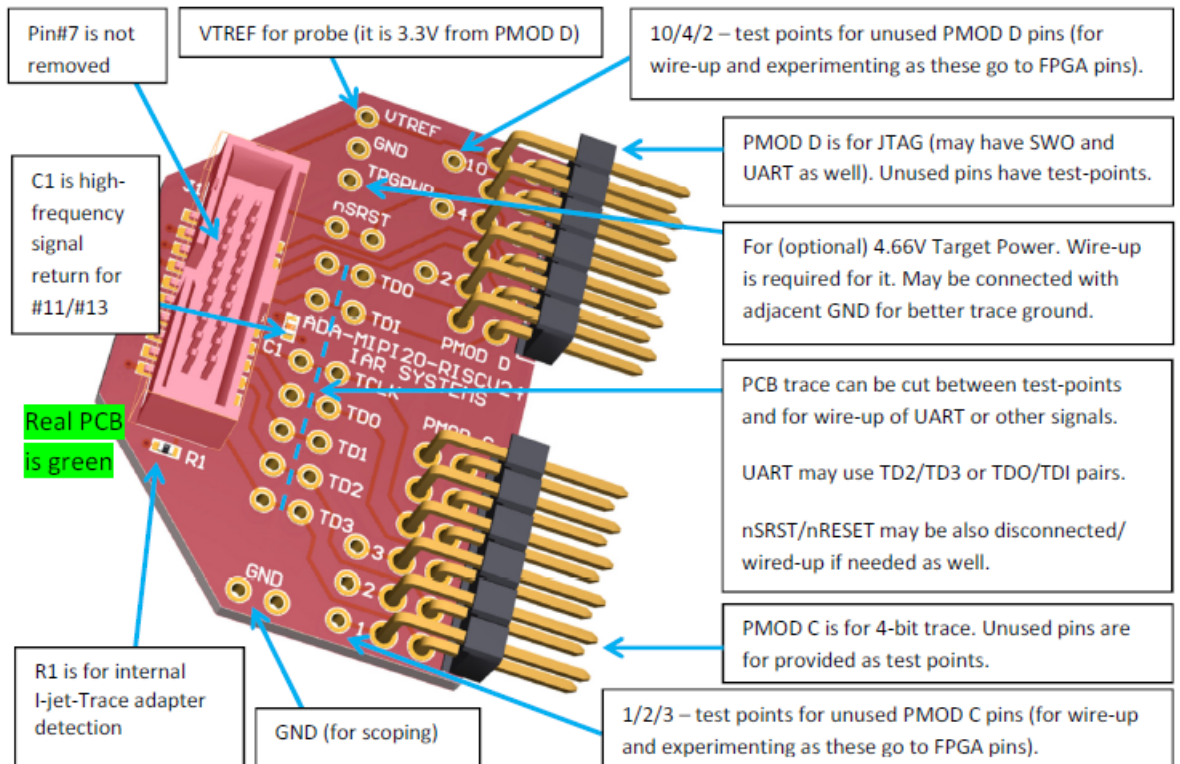
Table 23: ADA-MICTOR-MIP160 adapter pinout

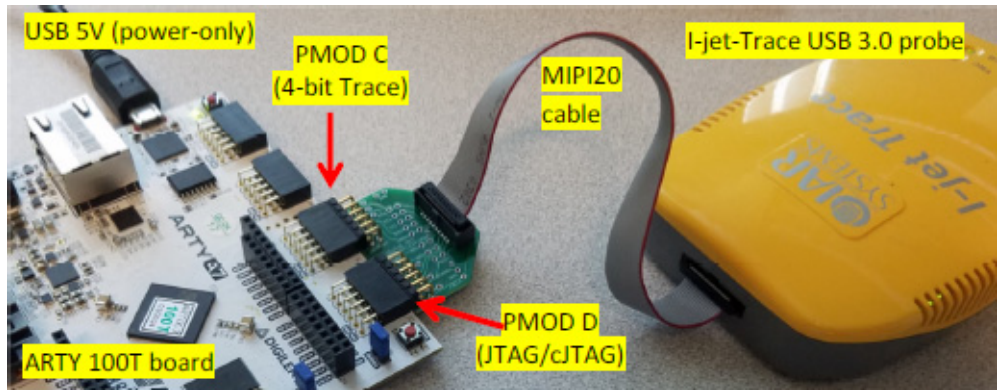
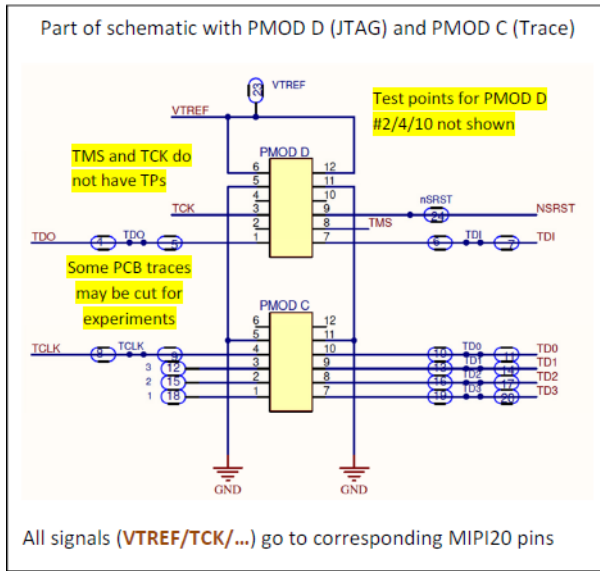
Signal	Pin	Pin	Signal
nTRST	9	10	DBGRO
DBGACK	11	12	VREF TRACE
TRACECLK	13	14	
GND	15	16	GND
TRACECTL	17	18	
TRACEDATA[00]	19	20	
TRACEDATA[01]	21	22	
TRACEDATA[02]	23	24	
TRACEDATA[03]	25	26	
TRACEDATA[04]	27	28	
TRACEDATA[05]	29	30	
TRACEDATA[06]	31	32	
TRACEDATA[07]	33	34	
TRACEDATA[08]	35	36	
TRACEDATA[09]	37	38	
TRACEDATA[10]	39	40	
TRACEDATA[11]	41	42	
TRACEDATA[12]	43	44	
TRACEDATA[13]	45	46	
TRACEDATA[14]	47	48	
TRACEDATA[15]	49	50	
	51	52	
	53	54	
	55	56	
GND	57	58	GND
GND	59	60	

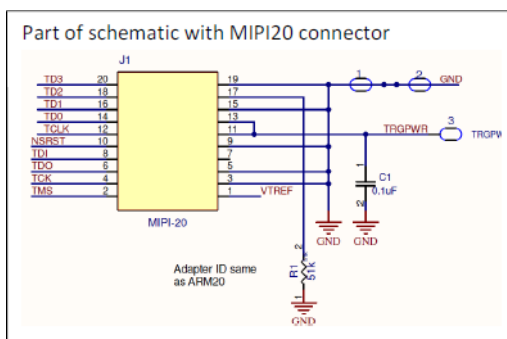
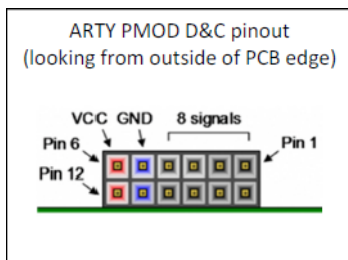
Table 23: ADA-MICTOR-MIP160 adapter pinout (Continued)

The ADA-MIPI20-RISCV24 adapter

The ADA-MIPI20-RISCV24 adapter converts the I-jet Trace CM standard MIPI-20 cable pinout to two Digilent Pmod connectors.







DESIGNING TARGET BOARDS FOR TRACE

Because trace port signals might have very fast rise and fall times—regardless of the trace frequency—it is important that the target PCB is designed properly so it does not distort the trace signals before they get to the connector.

For best results, it is recommended that the trace signals be simulated for signal integrity on a routed PCB by HyperLinx (or similar signal integrity SW).

Such SI tools will take into consideration the output impedance and rise and fall times of the MCU trace port lines, the length, geometry, and impedance of the PCB traces, the geometry of the layer stack as well as the dielectric properties of the PCB materials to give a simulated graph of the resulting waveform at the trace connector or any other place along the path.

If the resulting waveform is distorted, most simulation tools will help to determine the optimal series termination resistor for each trace line.



Important: All trace data lines and trace clocks must have a series resistor placed near the MCU source pin. The resistor value will be determined by the simulation tools or can be found experimentally by examining the live signal with an oscilloscope at the trace connector.

GENERAL PCB LAYOUT GUIDELINES

4-bit ETM trace

Arm Cortex-M devices have only a 4-bit ETM trace port. These trace signals must be routed to the standard 0.05 in × 0.05 in (1.27 mm × 1.27 mm) MIPI-20 connector header.

The recommended part number for a 4-bit ETM+JTAG debug connector is SHF-110-01-L-D-SM by Samtec or any other compatible shrouded header. The header should be positioned relatively close to the MCU—not more than 3 inches (75mm)—so that the even pins face the MCU as they have active signals on them.

16-bit ETM trace

Most Arm Cortex-R and Cortex-A devices come with a 16-bit trace port. To accommodate faster speeds, the signals must be connected to a 38-pin Mictor connector, making sure the track lengths from the MCU are matched to be within 0.5 inches (12.5 mm) to minimize signal skew.

The recommended part number for a 16-bit ETM+JTAG debug connector is 5767110-1 from AMP/Tyco.

The Mictor connector is designed to carry high-speed signals (10 Gb/s) and has a characteristic impedance of 50 Ohm. To eliminate signal distortion, the ETM trace signals on PCB must also have 50 Ohm impedance. The connector should be placed relatively close to the MCU—not more than 3 inches (75mm).

N-Trace

For RISC-V N-Trace, the same guidelines as above apply for 1-, 2-, 4-, and 16-bit trace ports. For details, see the *RISC-V Trace Connectors Specification* from the RISC-V N-Trace Task Group.

PCB routing

These are useful hints for PCB routing:

- Use series termination
 - Place a series resistor on each trace signal near the source (MCU).
- Minimize crosstalk
 - Keep all high-speed (fast rise and fall times) signals away from other signals to minimize crosstalk. Take special care of the TRACECLK signal.
- Minimize signal skew
 - Keep the individual trace port track lengths to be within 0.5 inches (12.5mm) of each other.

- Match impedance

Make the trace signal impedance 50 Ohm to match the impedance of the debug connectors and the debug probes.
- Minimize signal vias and avoid track stubs.

They might cause impedance mismatch, signal reflections, and distortions.
- Avoid trace pin multiplexing

Multiplexing of the trace pins with other functions increases track lengths and adds capacitance and inductance and should be avoided. If multiplexing is required, the designer should add jumpers to disconnect the trace pins from the other logic in case the tracing signals are too distorted to function properly.
- Use ground and power planes

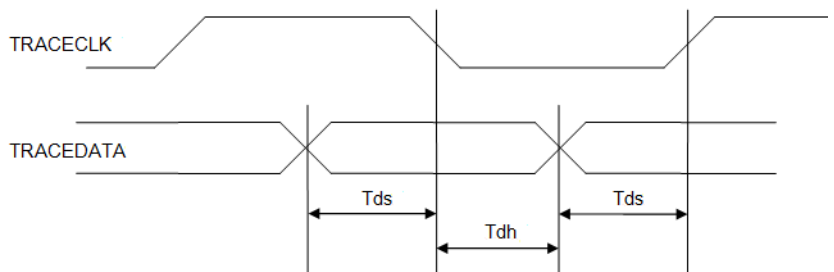
Using ground and power planes not only helps with power distribution, but also gives the high-speed signals the shortest return path to ground, which results in less signal loss. They also make the trace impedance matching easier and more consistent.

Trace signal requirements

I-jet Trace supports DDR (Double Data Rate) clocking mode, which means the data is output on both edges of the TRACECLK signal. To compensate for variations in MCU trace logic and target board PCB layouts, I-jet Trace contains logic to delay the TRACECLK and each TRACEDATA signal for up to 2.5 ns in 78 ps steps (78.125 ps steps to be exact). This logic is used to synchronize all trace data lines with the trace clock automatically to get the optimum trace data collection.

Data setup and hold

The following graph and table show the minimum setup and hold timing requirements of the trace signals with respect to TRACECLK. These timings are fixed by the MCU manufacturers, and might differ substantially from the data below, so are given as an example only.



Parameter	Value	Description
Tds	0.75 ns (minimum)	Data setup time
Tdh	0.75 ns (minimum)	Data hold time

Table 24: Data setup and hold times



Important: The minimum setup and hold times in the table are not as important as the length of the data valid time, because the logic inside the I-jet probe can delay the TRACECLK and TRACEDATA signals as needed, up to 2.5 ns. To get the best results, the trace valid data (Tds + Tdh) should be as long as possible. The best way to achieve that in the MCU or ASIC, is to make sure the trace data is changed in the middle of the High or Low DDR TRACECLK signal. This way the trace data valid time is the widest and the data setup and hold times are the biggest for a given frequency.

Switching thresholds

I-jet Trace measures the target signals reference voltage (V_{Tref}) at the debug connector and automatically adjusts its switching thresholds to $\frac{1}{2}$ of V_{Tref} . For example, on a 3.3 V target system, the switching thresholds are set to 1.65 V.